CLAIMS

What is claimed is:

1. In a microelectronic device, a structure on a substrate comprising:

a diffusion barrier layer disposed above and on the substrate, the diffusion barrier layer having a first thickness and a first dielectric constant;

an etch stop layer above and on the diffusion barrier layer, the etch stop layer having a second thickness and a second dielectric constant; and

an interlayer dielectric (ILD) layer disposed above and on the etch stop layer, wherein the structure has an effective dielectric constant in the range less than about 3.

2. The structure according to claim 1, wherein the diffusion barrier layer has a thickness in a range from about one atomic monolayer to about 2,500 Å.

3. The structure according to claim 1, wherein the diffusion barrier layer comprises an organic composition and wherein the etch stop layer comprises an inorganic composition.

4. The structure according to claim 1, wherein the diffusion barrier layer is selected from arylene, parylene and arylene ether polymers, and fluorinated polyimides.

5. The structure according to claim 1, wherein the diffusion barrier layer comprises an inorganic composition and wherein the etch stop layer comprises an organic composition.

6. The structure according to claim 1, wherein the etch stop layer comprises an organic composition and wherein the diffusion barrier layer is selected from silicon nitride, silicon oxide, silicon oxynitride, aluminum oxide, aluminum nitride, aluminum oxynitride, beryllium oxide, beryllium nitride, beryllium oxynitride, boron oxide, boron nitride, boron oxynitride, cerium oxide, cerium nitride, cerium oxynitride, yttrium oxide, yttrium nitride, yttrium oxynitride, carbon-doped oxide, carbon nitride, carbon oxynitride, a ceramic dielectric, and combinations thereof.

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7. The structure according to claim 1, further comprising:

an electrically conductive trace disposed in the substrate; and

a contact disposed in a recess that extends through the ILD layer, the etch stop layer, and the diffusion barrier layer, and wherein the contact makes an electrical connection to the trace.

8. The structure according to claim 1, further comprising:

an electrically conductive trace disposed in the substrate; and

a contact disposed in a recess that extends through the ILD layer, the etch stop layer, and the diffusion barrier layer, and wherein the contact makes an electrical connection to the trace, wherein the contact is a single-damascene contact article.

9. In a microelectronic device, a structure comprising:

a substrate having an upper surface;

an electrically conductive trace in the substrate;

a diffusion barrier layer above and on the substrate and the trace;

an etch stop layer above and on the diffusion barrier layer; and

an ILD layer disposed above and on the etch stop layer, wherein the diffusion barrier layer and the etch stop layer are mutually exclusively selected from either an organic composition or an inorganic composition.

10. The structure according to claim 9, wherein the trace surface is coplanar to the upper surface.

11. The structure according to claim 9, wherein the diffusion barrier layer has a thickness in a range from about one atomic monolayer to about 2,500 Å.

12. The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient less than about 3.

13. The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient of about 2.8.

14. The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient in a range from about 2.6 to about 2.8

15. The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient that is about 2.8

16. An article of manufacture comprising:

a semiconductor substrate;

a first dielectric layer disposed on the semiconductor substrate;

a second dielectric layer disposed on the first layer;

an interlayer dielectric (ILD) layer disposed on the second layer; and

a conductive damascene article, wherein the conductive damascene article is in contact with the substrate, the first dielectric layer, the second dielectric layer, and the ILD layer;

and wherein the first dielectric layer is an inorganic composition, and wherein the second dielectric layer is an organic composition.

17. The article of claim 16, wherein the first dielectric layer is selected from silicon nitride, silicon oxide, silicon oxynitride, aluminum oxide, aluminum nitride, aluminum oxynitride, beryllium oxide, beryllium nitride, beryllium oxynitride, boron oxide, boron nitride, boron oxynitride, cerium oxide, cerium nitride, cerium oxynitride, yttrium oxide, yttrium nitride, yttrium oxynitride, carbon-doped oxide, carbon nitride, carbon oxynitride, a ceramic dielectric, and combinations thereof.

18. The article of claim 16, wherein the second dielectric layer is selected from arylene, parylene and arylene ether polymers, and fluorinated polyimides.

19. The article of claim 16, wherein the second dielectric layer has a dielectric constant in a range of less than about 2.8.

20. The article of claim 16, wherein the second dielectric layer has a dielectric constant of about 2.

21. A process of making a structure, comprising:

forming an diffusion barrier layer in a substrate;

forming an etch stop layer above and on the diffusion barrier layer;

forming an ILD layer above and on the etch stop layer; and

forming a first recess in the ILD layer that exposes at least a part of the substrate, and wherein the diffusion barrier layer and the etch stop layer are mutually exclusively selected from either an organic composition or an inorganic composition.

22. The process according to claim 21, further comprising:

forming an antireflective coating (ARC) layer above and on the ILD layer;

patterning the ARC layer;

forming a second recess in the ARC and the ILD layer, wherein the second recess at least partially intersects the first recess, and wherein the second recess is wider than the first recess; and

filling the first and second recess with a metal.

23. The process according to claim 21, further comprising:

oxidizing the ARC layer; and

removing the ARC layer.

24. The process according to claim 21, wherein the ARC layer is selected from an organic composition and an inorganic composition.

25. The process according to claim 21, further comprising:

forming a trace in the substrate, wherein the substrate has an upper surface and wherein the trace has a trace surface that is coplanar with the upper surface.

26. The process according to claim 21, further comprising:

forming a trace in the substrate, wherein the substrate has an upper surface and wherein the trace has a trace surface that is coplanar with the upper surface; and

filling the first recess with a metal.

27. The process according to claim 21, further comprising:

forming a trace in the substrate, wherein the substrate has an upper surface and wherein the trace has a trace surface that is coplanar with the upper surface;

forming an antireflective coating (ARC) above and on the ILD layer;

patterning the ARC;

forming a second recess in the ARC and the ILD layer, wherein the second recess at least partially intersects the first recess, and wherein the second recess is wider than the first recess; and

filling the first and second recess with a metal.